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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,395	01/20/2004	Tom E. Burton	42P8329D2	3296

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
PASIA, REDENTOR M	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
06/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,395	BURTON ET AL.	
	Examiner	Art Unit	
	Redentor M. Pasia	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an

invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 19 and 20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,778,548 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

As to claim 19 of the application, claim 1 (of US 6,778,548 B1) shows a plurality of micro-engines to receive payload data from a memory controller (col. 12, lines 8-9); a transmit cell FIFO to build a packet header based on payload data received from the plurality of micro-engines or directly from a memory controller (col. 12, lines 12-14); the transmit cell FIFO including buffer control logic to receive packet data from the memory controller and place it in a cell buffer FIFO (col. 12, lines 20-23); the transmit cell FIFO also including: a cell buffer byte alignment circuit to track a start lane in the cell buffer FIFO indicating the start of free space in the cell buffer FIFO, determine a starting lane for the packet payload so that alignment of the payload data matches the start lane for the cell buffer FIFO (col. 12, lines 40-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuitries of the

reference by setting the circuitries up in order as discussed in the application in order to have an efficient way of utilizing memory allocations in a system.

As to claim 20 of the application, claim 1 (of US 6,778,548 B1) shows a address and write enable logic to synchronize the receipt of the packet header from the plurality of micro-engines and the packet payload from the memory controller and place both the packet header and the packet payload into the cell buffer FIFO; cell buffer read logic to transfer the packet header and packet payload data from the cell buffer FIFO to a destination specified by the packet header (col. 12, lines 26-33). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the logic of the reference by having the logic available to the second circuitry as mentioned in the application, in order to have proper packet transmission in a system.

Claims 19 and 20 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 (as to claim 19 of application) and claim 3 (as to claim 20 of application) of copending Application No. US 2004/0151176 A1. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

As to claim 19 of application, claim 4 (of US 2004/0151176 A1) shows a plurality of micro-engines to receive payload data from a memory controller; a transmit cell FIFO circuit adapted to build a packet header based on payload

data received from the plurality of micro-engines or directly from the memory controller and store payload data in a buffer; a cell buffer byte alignment circuit to track a start lane in the cell buffer FIFO indicating the start of free space in the cell buffer FIFO, determine a starting lane for the packet payload so that alignment of the payload data matches the start lane for the cell buffer FIFO (page 7; claims 4 and 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuitries of the reference by setting the circuitries up in order as discussed in the application in order to have an efficient way of utilizing memory allocations in a system.

As to claim 20 of application, claim 3 (of US 2004/0151176 A1) shows a address and write enable logic circuit to synchronize the receipt of the packet header from the plurality of micro-engines and the packet payload from the memory controller and place both the packet header and the packet payload into the cell buffer FIFO; a cell buffer read logic circuit to transfer the packet header and packet payload data from the cell buffer FIFO to a destination specified by the packet header (page 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the logic of the reference by having the logic available to the second circuitry as mentioned in the application, in order to have proper packet transmission in a system.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi (US 598541; hereinafter Malladi) in view of Richards et al. (US 6801535 B1; hereinafter Richards).

As to claim 19, Malladi shows a device comprising: a first circuitry to generate a packet header based on payload data received from a micro-engine or from a memory controller, the first circuitry comprising: second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in the first-in-first-out (FIFO) circuitry (figure 3 and 5; col. 7, line 30 to col. 8, line 15). However, Malladi does not show a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in FIFO circuitry, and to determine a starting lane for packet payload such that the alignment of payload data matches the start lane in the FIFO circuitry.

Richards shows a circuitry (processor 12) to track a start lane in the FIFO circuitry indicating a start of free space in FIFO circuitry (figure 10), and to determine a starting lane for packet payload such that the alignment of payload data matches the start lane in the FIFO circuitry (figures 8 -11; col. 3, lines 36-60; col. 10 lines 19-55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of Malladi by having the memory management of Richards as discussed above in order to have proper memory management and data transmission.

As to claim 20, the modified Malladi shows a logic to synchronize receipt of the packet header from the micro-engine and the packet payload from the memory controller, to store the packet header in the FIFO circuitry, and to transfer the packet header and packet payload data from the FIFO circuitry to a destination specified in the packet header (Figure 6; col. 8, lines 15-67).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Delvaux et al. (US 6490639 B1) – note abstract;

Karlsson et al. (US 7215670 B1) – note abstract;

Lincoln et al. (US 6829240 B1) – note abstract;

Gotesman et al. (US 6097734) – note abstract;

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Redentor M. Pasia whose telephone number is 571-272-9745. The examiner can normally be reached on M-F 7:30am to 5:00pm EST, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H. To can be reached on (571)272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Redentor Pasia

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600